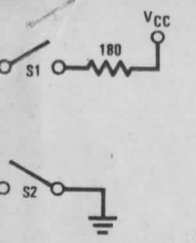


osed except where shown.

t Circuit

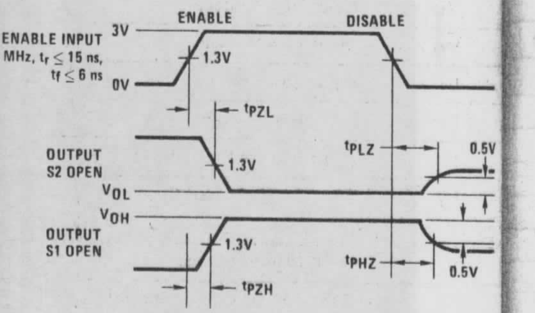
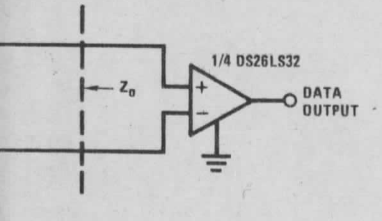


FIGURE 3. Enable and Disable Times

em, RS-422



DS26LS32C/DS26LS32M, DS26LS32AC, DS26LS33C/DS26LS33M, DS26LS33AC Quad Differential Line Receivers

General Description

The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have an input sensitivity of 200 mV over the input voltage range of ± 7V and the DS26LS33 and DS26LS33A have an input sensitivity of 500 mV over the input voltage range of ± 15V.

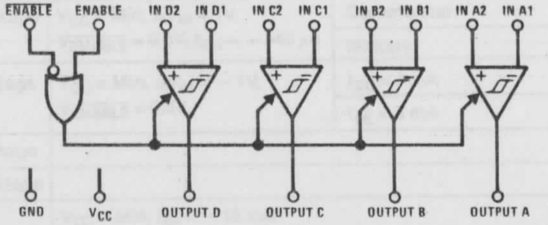
Both the DS26LS32A and DS26LS33A differ in function from the popular DS26LS32 and DS26LS33 in that input fail-safe circuitry is provided for each receiver, which causes the outputs to go to a logic "1" state when the inputs are open.

Each version provides an enable and disable function common to all four receivers and features TRI-STATE® outputs with 8 mA sink capability. Constructed using low power Schottky processing, these devices are available over the full military and commercial operating temperature ranges.

Features

- High differential or common-mode input voltage ranges of ± 7V on the DS26LS32 and DS26LS32A and ± 15V on the DS26LS33 and DS26LS33A
- ± 0.2V sensitivity over the input voltage range on the DS26LS32 and DS26LS32A, ± 0.5V sensitivity on the DS26LS33 and DS26LS33A
- Input fail-safe circuitry on the DS26LS32A and DS26LS33A
- DS26LS32 and DS26LS32A meet all requirements of RS-422 and RS-423
- 6k minimum input impedance
- 100 mV input hysteresis on the DS26LS32 and DS26LS32A, 200 mV on the DS26LS33 and DS26LS33A
- Operation from a single 5V supply
- TRI-STATE drive, with choice of complementary output enables for receiving directly onto a data bus
- Pin replacement for Advanced Micro Devices AM26LS32

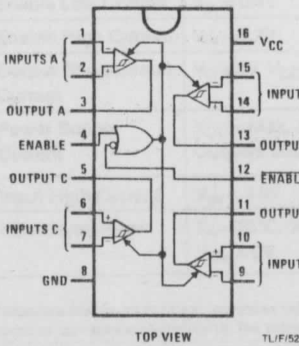
Logic Diagram



TL/F/5255-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5255-2

Truth Table

ENABLE	$\overline{\text{ENABLE}}$	Input	Output
0	1	X	Hi-Z
See Note Below		$V_{ID} \geq V_{TH}$ (Max)	1
		$V_{ID} \leq V_{TH}$ (Min)	0
		Open	1*

Hi-Z = TRI-STATE

* DS26LS32A and DS26LS33A only

Note: Input conditions may be any combination not defined for ENABLE and $\overline{\text{ENABLE}}$.

Order Number DS26LS32MJ, DS26LS32CJ, DS26LS32CN, DS26LS32ACJ, DS26LS32ACN, DS26LS33MJ, DS26LS33CJ, DS26LS33CN, DS26LS33ACJ or DS26LS33ACN
See NS Package J16A or N16A

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	Min	Max	Units
(V_{CC}) DS26LS33M	4.5	5.5	V
DS26LS33C , DS26LS33AC	4.75	5.25	V
) DS26LS33M	− 55	+ 125	°C
DS26LS33C , DS26LS33AC	0	+ 70	°C

ss otherwise specified (Notes 2, 3 and 4)

	Min	Typ	Max	Units
+ 7V	− 0.2	± 0.07	0.2	V
≤ + 15V	− 0.5	± 0.14	0.5	V
	6.0	8.5		kΩ
			2.3	mA
			− 2.8	mA
	2.7	4.2		V
	2.5	4.2		V
			0.4	V
			0.45	V
			0.8	V
	2.0			V
			− 1.5	V
			20	μA
			− 20	μA
			− 0.36	mA
			20	μA
	− 15		− 85	mA
32A		52	70	mA
33A		57	80	mA
			100	μA
32A		100		mV
33A		200		mV

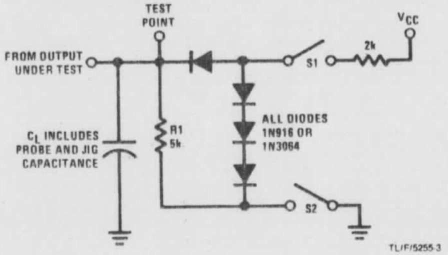
be guaranteed. They are not meant to imply that the s for actual device operation.

egative; all voltages are referenced to ground, unless

Parameter		Conditions	DS26LS32/DS26LS33			DS26LS32A/DS26LS33A			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PLH} t_{PHL}	Input to Output	$C_L = 15$ pF		17 17	25 25		23 23	35 35	ns ns
t_{LZ} t_{HZ}	ENABLE to Output	$C_L = 5$ pF		20 15	30 22		15 20	22 25	ns ns
t_{ZL} t_{ZH}	ENABLE to Output	$C_L = 15$ pF		15 15	22 22		14 15	22 22	ns ns

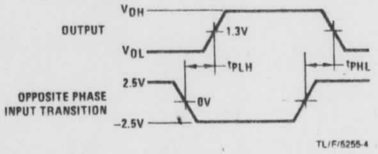
AC Test Circuit and Switching Time Waveforms

Load Test Circuit for TRI-STATE Outputs


TEST POINT
V_CC
FROM OUTPUT UNDER TEST
2k
S1
C_L INCLUDES PROBE AND JIG CAPACITANCE
R1 5k
ALL DIODES 1N916 OR 1N3064
S2

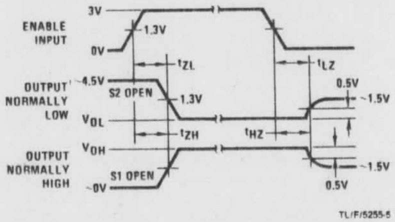
TL/F/5255-3

Propagation Delay (Notes 1 and 3)



TL/F/5255-4

Enable and Disable Times (Notes 2 and 3)



TL/F/5255-5

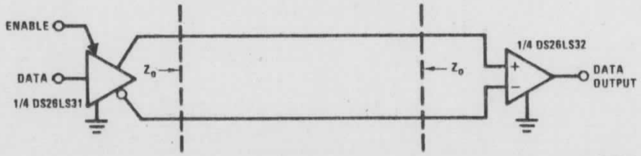
Note 1: Diagram shown for $\overline{\text{ENABLE}}$ low.

Note 2: S1 and S2 of load circuit are closed except where shown.

Note 3: Pulse generator for all pulses: Rate ≤ 1.0 MHz; $Z_O = 50\Omega$; $t_r \leq 15$ ns; $t_f \leq 6.0$ ns.

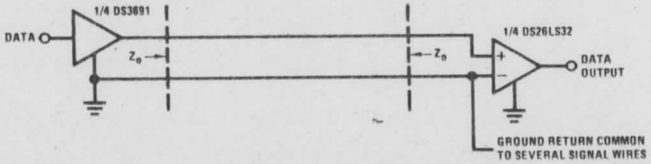
Typical Applications

Two-Wire Balanced Systems, RS-422



TL/F/5255-6

Single Wire with Common Ground Unbalanced Systems, RS-423



TL/F/5255-7

National Semiconductor

DS26LS31C/DS26LS31M Quad High Speed Differential Line Driver

General Description

The DS26LS31 is a quad differential line driver designed for digital data transmission over balanced lines. The DS26LS31 meets all the requirements of EIA Standard RS-422 and Federal Standard 1020. It is designed to provide unipolar differential drive to twisted-pair or parallel-wire transmission lines.

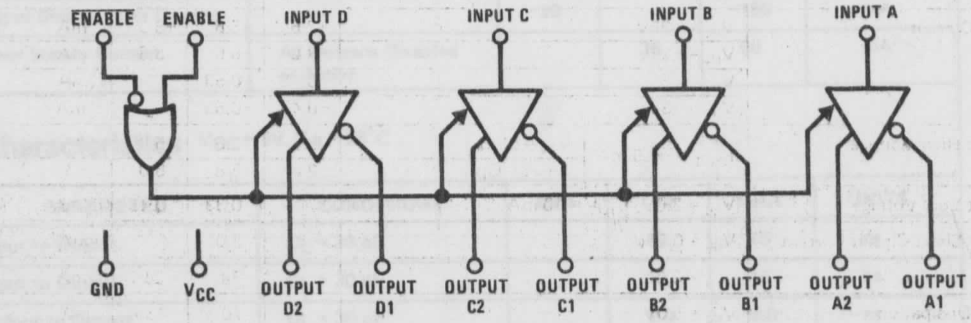
The circuit provides an enable and disable function common to all four drivers. The DS26LS31 features TRI-STATE® outputs and logically ANDed complementary outputs. The inputs are all LS compatible and are all one unit load.

The DS26LS31 features a power up/down protection circuit which TRI-STATEs the outputs during power up or down preventing erroneous glitches on the transmission lines.

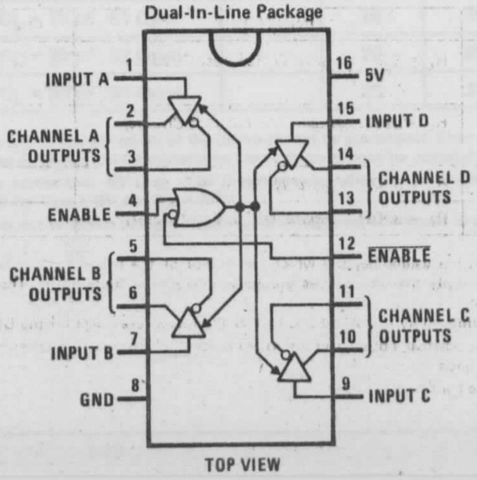
Features

- Output skew – 2.0 ns typical
- Input to output delay – 10 ns
- Operation from single 5V supply
- 16-pin hermetic and molded DIP package
- Outputs won't load line when $V_{CC} = 0$
- Four line drivers in one package for maximum package density
- Output short-circuit protection
- Complementary outputs
- Meets the requirements of EIA Standard RS-422
- Pin compatible with AM26LS31
- Available in military and commercial temperature range
- Glitch free power up/down

Logic Diagram



Connection Diagram



Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	7V
Output Voltage	5V
Output Voltage (Power OFF)	−0.25V to 6V
Maximum Power Dissipation* at 25°C	
Cavity Package	1509 mW
Molded Package	1476 mW

*Derate cavity package 10.1 mW/°C above 25°C; derate molded package 11.9 mW/°C above 25°C.

Electrical Characteristics (Notes 2, 3 and 4)

PARAMETER		CONDIT
V_{OH}	Output High Voltage	$I_{OH} = -20$ m
V_{OL}	Output Low Voltage	$I_{OL} = 20$ mA
V_{IH}	Input High Voltage	
V_{IL}	Input Low Voltage	
I_{IL}	Input Low Current	$V_{IN} = 0.4V$
I_{IH}	Input High Current	$V_{IN} = 2.7V$
I_I	Input Reverse Current	$V_{IN} = 7V$
I_O	TRI-STATE Output Current	V V
V_{CL}	Input Clamp Voltage	$I_{IN} = -18$ m
I_{SC}	Output Short-Circuit Current	
I_{CC}	Power Supply Current	All Outputs or Active

Switching Characteristics $V_{CC} = 5V, T_A = 25°C$

PARAMETER		CONDI
t_{PLH}	Input to Output	$C_L = 30$ pF
t_{PHL}	Input to Output	$C_L = 30$ pF
Skew	Output to Output	$C_L = 30$ pF
t_{LZ}	Enable to Output	$C_L = 10$ pF
t_{HZ}	Enable to Output	$C_L = 10$ pF
t_{ZL}	Enable to Output	$C_L = 30$ pF
t_{ZH}	Enable to Output	$C_L = 30$ pF

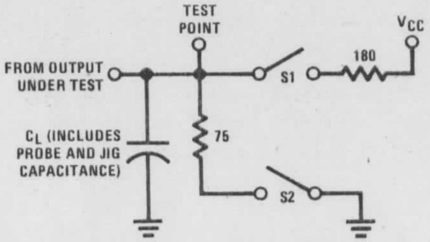
Note 1: "Absolute Maximum Ratings" are those values beyond which t that the devices should be operated at these limits. The tables of "Electri

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C range for the DS26LS31. All typicals are given for V_{CC} =

Note 3: All currents into device pins are positive; all currents out of dev specified.

Note 4: Only one output at a time should be shorted.

AC Test Circuit and Switching Time Waveforms



Note. S1 and S2 of load circuit are closed except where shown.

FIGURE 1. AC Test Circuit

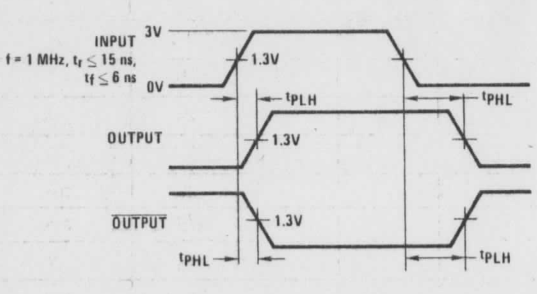


FIGURE 2. Propagation Delays

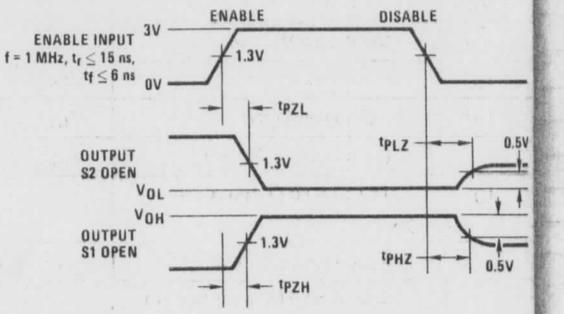
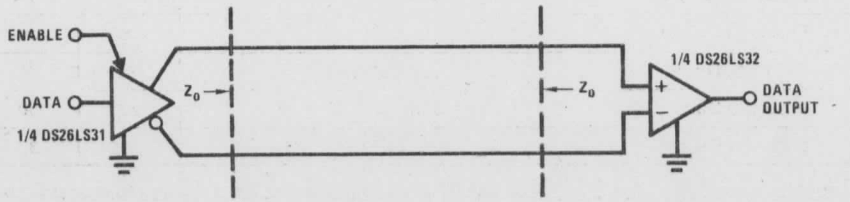


FIGURE 3. Enable and Disable Times

Typical Applications

Two-Wire Balanced System, RS-422



National Semiconductor

DS26LS32C/DS26LS32M, DS2
DS26LS33C/DS26LS33M, DS2
Quad Differential Line Receiv

General Description

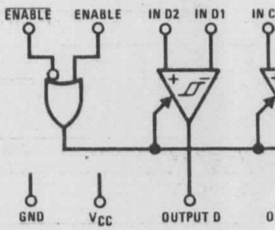
The DS26LS32 and DS26LS32A are quad differential line receivers designed to meet the RS-422, RS-423 and Federal Standards 1020 and 1030 for balanced and unbalanced digital data transmission.

The DS26LS32 and DS26LS32A have an input sensitivity of 200 mV over the input voltage range of ±7V and the DS26LS33 and DS26LS33A have an input sensitivity o 500 mV over the input voltage range of ±15V.

Both the DS26LS32A and DS26LS33A differ in functio from the popular DS26LS32 and DS26LS33 in that inpu fail-safe circuitry is provided for each receiver, which causes the outputs to go to a logic "1" state when the inputs are open.

Each version provides an enable and disable functio common to all four receivers and features TRI-STATE® outputs with 8 mA sink capability. Constructed using low power Schottky processing, these devices are available over the full military and commercial operating temperature ranges.

Logic Diagram



Connection Diagram

Dual-In-Line Package